IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Daniel D'Souza

Serial No. :	09/918,183	**Group Art Unit :**	2829
Filed :	July 30, 2001	**Examiner :**	Patel, Paresh
For :	Wafer Level Dynamic Burn In	**Atty Docket :**	/ 00-464

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Mark Salvatore

January 8, 2004 Mark Salvatore

Date Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

Date: 6 JAN 04